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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/660,926	09/13/2000	Nobuaki Tokushige	900-348	7467

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EXAMINER
HU, SHOUXIANG

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/06/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/660,926	TOKUSHIGE, NOBUAKI	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication app ars on th cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 May 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-11 and 22-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-11 and 22-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *28 May 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 5/28/02 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Claim Objections

2. Claims 22- 24, insofar as being supported by elected Species I along with Species II, are objected to because of the following informalities or defects:

In claims 22-24, the term of "depleted simultaneously" should read as -- depleted simultaneously in the standby state--.

Claim 24 recites the subject matter that the P-type well and the N-type well are electrically isolated from each other. However, according to Fig. 4(d), these wells are only substantially electrically isolated from each other under certain bias polarities with respect to these wells.

In addition, in claim 24, the term of "standby" should read as –standby state--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 5, 6, 9 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 5 and 9 both recite an N-type and a P-type transistors, but they both fail to clarify whether their respectively claimed semiconductor devices have a single transistor or have two transistors simultaneously.

Both claims 4 and 8 recite a limitation that the well has a first conductivity type same as the one of the substrate directly under the well. However, each of their respective dependent claims 5 and 6, and, 9 and 10, recites an N-type and a P-type wells, and one of these two opposite-type wells formed in a same substrate would contradict to that limitation recited in claims 4 and 8.

Furthermore, in claims 6 and 9, it is not clear what are the correlations among the "plurality of wells", "the P-type well" and "the N-type well".

5. Claims 22 and 23 are rejected as they each recite the limitation "said MOS transistors". There is insufficient antecedent basis for this limitation in their corresponding independent claims 1 and 7. Each of claims 1 and 7 only defines a single transistor with a diffusion layer or well having a same conductivity type as the one of the substrate.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 7-10, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Burr (6,072,217) in view of Numata et al. ("Numata"; 6,043,536).

Burr discloses a semiconductor device (Figs. 5-7), comprising: a MOS transistor on a semiconductor layer (including 516) formed on a semiconductor substrate (510); buried insulating film (508); an element isolating region (Ox); and a contact potion (544 or 546) for applying a bias voltage to a P-type well (540) or N-type well (542) in the substrate, wherein the P-type well and the N-type well are substantially electrically isolated from each other, and the P-type well (540) is of the first conductivity type same as one of the other region of the semiconductor substrate directly under the well.

Burr does not expressly disclose that the bias voltage can be applied to the P-type or N-type well through a contact region formed in the element isolating region. However, Numata teaches to form an SOI type MOS transistor (Fig. 20, or 41) with a bias voltage (10) applied to the back gate well (11) in the substrate through a contact region (19) formed in an element isolating region (12), for supplying the bias voltage from the upper surface of the substrate.

Therefore, it would have been obvious to one of ordinary skilled in the art at the time the invention was made to make the semiconductor device of Burr with each of the bias voltages being applied to the corresponding back-gate well through a contact region formed in the element isolating region, as taught in Numata, so that a semiconductor device with the bias voltages being supplied from the front surface of the substrate would be obtained.

8. Claims 1, 4-6, 11 and 22-24, insofar as being in compliance with 35 U.S.C. 112, and as being best understood in view of the claim objection above, are rejected under 35 U.S.C. 103(a) as being unpatentable over Burr (6,072,217) in view of Numata et al. ("Numata"; 6,043,536) as applied to claims 7-10 above, and further in view of Yamaguchi et al. ("Yamaguchi"; 5,557,231).

The disclosures of Burr and Numata are discussed as applied to claims 7-10 above.

Regarding claims 1, 4-6 and 22, it is first noted that, although Burr does not expressly disclose that the well (540 or 542) in the embodiments of Figs. 5-7 can underlie at least the entire source, drain and channel regions, one of ordinary skill in the art would readily recognize that the well in Burr functions as a back gate; that the function between the performance of the transistor and its underlying back gate mainly depends on the portion of the back gate that directly overlaps with the channel region as the source and drain regions are always highly conductive; and that the back gate in the art can readily be wide enough to undrlie at least the entire source, drain and channel regions for the convenience

of forming the contact to the back gate and for easing process conditions such as alignment requirement between the back gate and the channel region, as evidenced in Numata (see the back gate 11 in Figs. 20 and 41). Hence, it would have been obvious to one of ordinary skilled in the art at the time the invention was made to make the above semiconductor device collectively taught by Burr and Numata with the back gate underlying at least the entire source, drain and channel regions, per the further teachings of Numata, so that a semiconductor device with improved design and process convenience and easefulness for forming the well and the well contact would be obtained.

Regarding claims 1, 4, 5, 6, 11 and 22-24, although Burr and Numata do not disclose that different bias voltages are applied to the substrate in an operating state and a standby state, Yamaguchi teaches (see the abstract, and also see Figs. 2, 16 -18) that by changing the potential of the substrate bias in the active state and the standby state of a MOS transistor, which inherently changes the threshold voltage of the MOS transistor, the power consumption in the standby state can be reduced and the speed of operation in the active state can be improved.

It would therefore have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the different bias voltages of Yamaguchi into the semiconductor device collectively taught by Burr and Numata, so that a semiconductor device with reduced power consumption in the standby state and improved operation speed in the active state would be achieved.

Regarding claims 22-24, it is further noted that the device of Burr (Figs. 5-7) comprises an nMOSFET and a pMOSFET overlying the P-type well (540) and the N-type well (542), respectively; and Yamaguchi further teaches to form a pair of nMOSFET and pMOSFET (see Fig. 16-18) being both fully depleted in the standby state simultaneously (see col. 14, lines 35-63) for further reducing energy consumption.

It would therefore have been obvious to one of ordinary skill in the art at the time the invention was made to make the semiconductor device collectively taught by Burr, Numata and Yamaguchi with the nMOSFET and pMOSFET being both fully depleted in the standby state simultaneously, so that the energy consumption can be further reduced, per the further teachings of Yamaguchi.

Response to Arguments

9. Applicant's arguments filed on May 28, 2002, have been fully considered but they are not persuasive.

Applicant's main arguments include: (A) The applied prior art references do not teach the claim invention of claim 7 because Burr does not teach to form a well contact using an isolation region and its well is too small to be connected, and that Numata does not teach to form wells that are adapted to the conductivity types of the transistors; (B) There is no suggestion to combine the references; and (D) Yamaguchi fails to teach simultaneous full depletion of P- and N-channel transistors.

In response to Applicant's argument (A), which is against the references individually, it is noted that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, what applicant argues is not shown by one reference is clearly taught by the other. Burr discloses the claimed invention (claim 7) including the wells that are adapted to the conductivity types of the transistors, except that Burr does not expressly discloses that each of these back-gate wells can be expanded and connected to a well contact through an isolation region. Numata is relied on for showing that it was known in the art that a back-gate well can be readily expanded and connected to a well contact through an isolation region, regardless whether or not Numata teaches the adaptability of the wells to the conductivity types of the transistors. Accordingly, all of the claimed elements (in claim 7) are clearly present in the collective teachings of Burr and Numata.

Regarding Applicant's argument (B), the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Burr discloses the claimed invention (claim 7) including the wells that are adapted to the

conductivity types of the transistors, except that Burr does not expressly discloses that each of these back-gate wells can be expanded and connected to a well contact through an isolation region. And, as evidenced in Numata, one of ordinary skill readily recognize that each of such back-gate wells can be readily expanded and connected to a well contact through an isolation region; and that the fact that the back-gate well and substrate in Numata are of opposite conductivity types would not constitute a teaching away from Burr because: (1) Numata does teach that the back-gate well and substrate cannot be of a same conductivity; (2) Burr teaches to form two opposite types of MOSFETs, one of which has a back-gate well of a conductivity type opposite to that of the substrate, just as what as in the case of Numata, thus the other resulting back gate well has to be of a same conductivity type as the substrate if the two back-gates are to be formed in the same substrate.

And, one of ordinary skill in the art would also readily recognize that the function between the performance of the transistor and its underlying back gate mainly depends on the portion of the back gate that directly overlaps with the channel region as the source and drain regions are always high conductive; and that the back gate in the art can readily be wide enough to underlie at least the entire source, drain and channel regions for the convenience of forming the contact to the back gate and for easing process conditions such as alignment requirement between the back gate and the channel region, as evidenced in Numata (see the back gate 11 in Figs. 20 and 41). Hence, it would have been obvious to one of ordinary skilled in the art at the time the invention was made to

make the semiconductor device of Burr with the back-gate wells being expanded to underlie at least the entire source, drain and channel regions and connected to a well contact through an isolation region, per the teachings of Numata, so that a semiconductor device with desired back-gate electrodes and improved design and process convenience and easefulness would be obtained.

With respect to Applicant's argument (C), it is noted that Yamaguchi does specifically teach simultaneous full depletion of the P- and N-channel transistors (see Figs. 16-18, also col. 14, lines 35-63).

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 or 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ***Shouxiang Hu*** whose telephone number is **(703) 306-5729**. The examiner can normally be reached on Monday through Thursday from 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, ***Tom Thomas***, can be reached on **(703) 308-2772**. The appropriate fax phone number for the organization where this application or proceeding is assigned is **(703) 308-7724**.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **(703) 308-0956**.

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

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August 1, 2002